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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,736	02/14/2002	Mark Champion	72704	3479

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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 05/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,736	CHAMPION, MARK	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-14 and 16* is/are rejected.

7)☒ Claim(s) *8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3,4, 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statements (IDS) submitted on April 9, 2002, February 17, 2004, February 12, 2004, and April 19, 2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

Figures 1A, 1B, and 1C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-7, 12-14, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Ansari (US# 6,665,749).

Regarding claim 1, Ansari teaches a **memory device** (the entire system of Figure 2, where the system comprises a processor, memory, and memory controller) **with a memory array** [DRAM (210)] **where the memory is divided into pages** (col. 7, lines 50-52) **and each memory location has a row and column address** (col. 7, line 66 - col. 8, lines 5). The **row decoder connected to the memory array for selection a row address and column decoder connected to the memory array for selecting a column address in the memory array** corresponds to the memory controller (222) for accessing DRAM (210) (col. 8, lines 1-3). Ansari teaches **a multi-sequence address generator** [VTU (138) **that generates addresses** (col. 8, lines 15-22, 42-64 and line 66 – col. 9, line 3), **has a burst mode** (col. 3, lines 1-6), **and while in burst mode generates one or more burst sequences of address according to burst parameters, where each sequence has an index** (stride) **indicating the separation between two addresses in the sequence** (col. 8, line 18).

Regarding claim 4, Ansari teaches that **the row address indicates a page in memory, while the column address indicates a locating within the page** (col. 8, lines 3-5).

Regarding claim 5, Ansari teaches that the **multi-sequence address generator** (VTU) **supplies an address to the column decoder** (memory controller) (col. 13, line 58 – col. 14, line 1).

Regarding claim 6, Ansari teaches that **the burst parameters include a starting address, index parameter** (stride), **and burst length** (col. 8, lines 15-23).

Regarding claim 7, Ansari inherently teaches **that the index parameter** (stride) **is added to an address to create a burst sequence** according to the explanation of the index parameter (stride) in determining the final address and what the index parameter (stride) signifies (col. 8, lines 19-24 & col. 9, lines 10-11; col. 2, lines 17-22).

Regarding claim 12, Ansari **a memory array** [DRAM (210)] **where the memory is divided into locations** [pages (col. 7, lines 50-52)] **and each memory location has a row and column address** (col. 7, line 66 - col. 8, lines 5). Ansari teaches **an address generator** [VTU (138) **that generates addresses** (col. 8, lines 15-22, 42-64 and line 66 – col. 9, line 3), **and generates two or more burst sequences of address according to burst parameters, where each sequence has an index** (stride) **indicating the separation between two addresses in the sequence** (col. 8, line 18). Ansari inherently teaches **that the index parameter** (stride) **is added to an address** to create a burst sequence according to the explanation of the index parameter (stride) in determining the final address and what the index parameter (stride) signifies (col. 8,

lines 19-24 & col. 9, lines 10-11; col. 2, lines 17-22). Also, the claim limitation does not recite that the two sequences are generated simultaneously, and therefore the two sequences could be generated serially, like that of Ansari.

Regarding claim 13, Ansari teaches a **data system** [computer system (100); Fig. 1] **with a data source and a data destination** [VBP (208) and memory (210); Fig. 2] **that moves data between the two according to a data orders (1st and 2nd**, dependent upon the stride value; col. 13, line 66 – col. 14, line 7), as well as **a scan converter system** (where the system comprises a processor, memory, and memory controller) **with a memory array** [DRAM (210)] **where the memory is divided into pages** (col. 7, lines 50-52) **and each memory location has a row and column address** (col. 7, line 66 - col. 8, lines 5). Ansari teaches **a multi-sequence address generator** [VTU (138) **that generates addresses** (col. 8, lines 15-22, 42-64 and line 66 – col. 9, line 3), **has a burst mode** (col. 3, lines 1-6), **and while in burst mode generates one of two burst sequences of address according to burst parameters, where each sequence has an index** (stride) **indicating the separation between two addresses in the sequence** (col. 8, line 18), which in turn defines **that the two burst sequences correspond to a respective data order** based on their stride.

Regarding claim 14, Ansari teaches **generating burst sequences of address**, where **the burst parameters include a starting address, index parameter** (stride) **that indicates an index** (stride), **and burst length** (col. 8, lines 15-23). Ansari teaches

a multi-sequence address generator [VTU (138) that generates addresses (col. 8, lines 15-22, 42-64 and line 66 – col. 9, line 3), has a burst mode (col. 3, lines 1-6), and while in burst mode **generates a burst sequence of addresses according the burst length, where the first address is the starting address and additional addresses are generated by adding the index to the previous address in the burst sequence.** Ansari inherently teaches **that the index parameter** (stride) **is added to an address to create a burst sequence** according to the explanation of the index parameter (stride) in determining the final address and what the index parameter (stride) signifies (col. 8, lines 19-24 & col. 9, lines 10-11; col. 2, lines 17-22).

Regarding claim 16, Ansari teaches that the **index parameter** (stride) **is an index** (stride) (col. 9, lines 10-11; col. 2, lines 17-22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ansari as applied to claims 1, 4-7, 12-14, and 16 above, and further in view of Lu (US# 6,023,745).

Regarding claim 2, Ansari recites DRAM memory use of pages, but fails to teach that the memory is comprised of two or more memory banks and that one page from each bank can be active at the same time. Lu teaches a **DRAM partitioned into a number of arrays**, such that for a **dual bank** access **a row (page) in each bank can be active at one time** (abs., lines 3-14). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Ansari and Lu before him at the time the invention was made to modify the burst system of Ansari to include the multi-bank access of Lu, because then access times approaching a peak bandwidth could be obtained (col. 6, lines 13-18).

Regarding claim 3, Ansari teaches **burst accessing**, but fails to teach that one page from each bank can be active at the same time. Lu teaches that **a first page can be accessed while a first page is being accessed** (abs., lines 3-14).

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ansari as applied to claims 1, 4-7, 12-14, and 16 above, and further in view of Chudnovsky et al. (US# 6,519,673).

Regarding claim 9, Ansari recites index (stride) use, but fails to teach that each sequence can have an index (stride) of one. Chudnovsky et al. teaches a multi-bank memory device that facilitates **sequences with an index of one** [stride 1 data access patterns) abs., lines 1-2]. Therefore it would have been obvious to one of ordinary skill

in the art having the teachings of Ansari and Chudnovsky et al. before him at the time the invention was made to modify the burst system of Ansari to include the index (stride) value of Chudnovsky et al., because then a system for addressing a multi-bank device would provide no bank conflicts, as taught by Chudnovsky et al. (abs., lines 4).

Regarding claim 10, Chudnovsky et al. teaches using a power of two stride index, such as that of eight for **sequences with an index value of eight** (abs., line 3).

Regarding claim 11, Chudnovsky et al. teaches using a power of two stride index, such as that of sixteen for **sequences with an index value of sixteen** (abs., line 3).

Allowable Subject Matter

Claims 8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related burst access systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to

4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

May 13, 2004

Brian R. Peugh
Patent Examiner
Art Unit 2187